Abstract of the Disclosure

Provided are a circuit and a method for transforming a data input/output format of a semiconductor memory device which is capable of generating various types of data patterns when the number of memory cells connected to one column selection line is greater than the number of data input pins. The circuit for transforming a data input/output format of a semiconductor memory device includes a first transmission circuit, a second transmission circuit, and a mode register set (MRS). The first transmission circuit is activated when a first test mode signal is enabled, receives n data inputs from n data input ends, and transmits the n data inputs to m memory cells. Here, n and m are natural numbers and m is greater than n. The second transmission circuit is activated when a second test mode signal is enabled, receives n data inputs from the n data input ends, and transmits the n data inputs to the m memory cells. The mode register set (MRS) receives a command and an address from outside the semiconductor device and outputs the first test mode signal and the second test mode signal according to combinations of the command and the address. In particular, data that is transmitted to adjacent memory cells of the m memory cells is inputted to different input ends of the n data input ends.

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